TELEDYNE LECROY
Everywhereyoulook™

Kibra™ 380
DDR3 Protocol Analyzer

DDR3 BUS & TIMING ANALYSIS

Key Features

- **Fast and Easy DDR3 Debug**
  - **— Self-contained system**
  - **— Fast & easy setup**
  - **— Impedance matched Interposer probing**
- **Comprehensive JEDEC Trigger and Capture**
  - **— Trigger on 43 JEDEC bus & timing violations**
  - **— Detect 12 DDR3 protocol violations**
  - **— Trigger on RD/WR to specific addresses**
  - **— Low latency trigger-out to scope for RD/WR**
- **Innovative Displays Focused on Timing Analysis**
  - **— Traditional State and Timing Waveform displays**
  - **— View Command metrics (per bank & rank)**
- **Flexible, Scalable Platform**
  - **— 4 GB memory for Extended recording**
  - **— Supports registered and unbuffered DIMM types**
  - **— Address multi-channel memory testing by cascading analyzers**
  - **— CrossSync™ allows synchronized views with other serial busses**

Teledyne LeCroy Kibra™ 380 DDR3 Protocol Analyzer

The Teledyne LeCroy Kibra 380 is a stand-alone DDR3 protocol analyzer that provides comprehensive DDR3 bus and JEDEC timing analysis. Small and portable, the Kibra 380 is controlled over USB using any Windows-based PC and offers state and timing waveform displays to allow fast debugging of DDR3 systems and memory controllers.

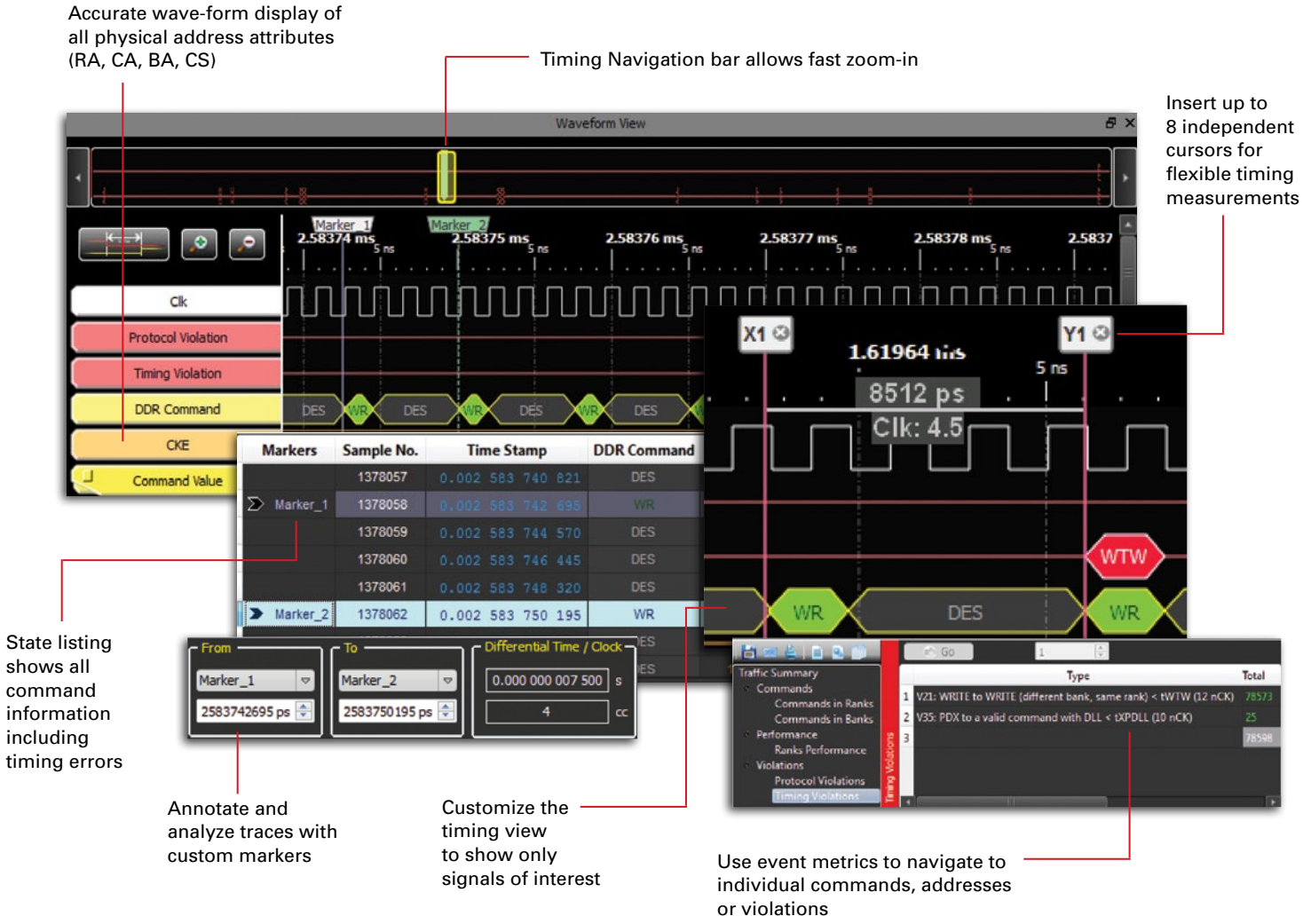
The cost and complexity of testing DDR3 is a major obstacle for validation teams struggling with monolithic test approaches that rely on JEDEC preprocessor hardware combined with costly logic analyzer platforms. The Kibra 380 is the first standalone bus analyzer that provides all the essential triggering of a JEDEC pre-processor while simultaneously capturing timing waveforms, decoded state listings, performance, and utilization statistics.

Using non-intrusive slot interposer probes, the system provides loss-less capture of address, command and control signals (ADD/CMD/CNTRL). By focusing on state-based capture and excluding the data signals, the Kibra 380 allows quick analysis of DDR3 transactions. Thanks to high impedance probing and specialized trigger logic, this self-contained solution can monitor a fully loaded quad rank memory bus and identify 65 JEDEC timing and command violations in real time. 4 GB of capture memory can record 8x the number of memory events compared to a typical logic analyzer.

Easy Setup — No Calibration Needed!

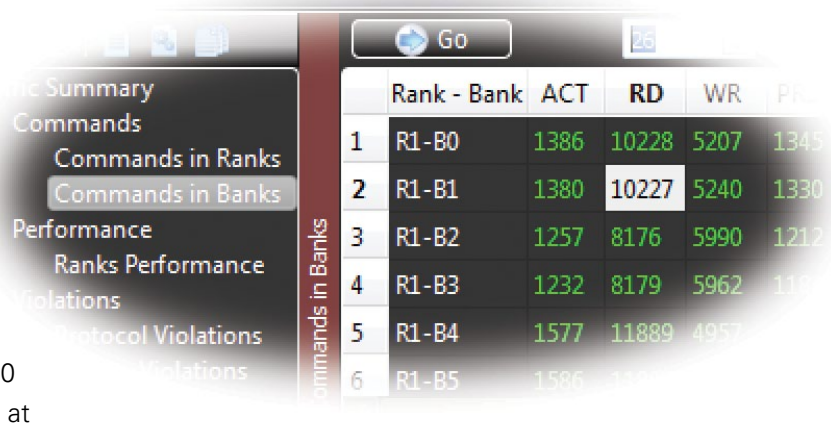
Start using the Kibra 380 immediately without time consuming calibration. Simply enter the memory controller parameters and start recording. The software will automatically load JEDEC trigger values for the DIMM type specified. Users can selectively disable or override any of the JEDEC triggers on-the-fly.

JEDEC timing values load automatically based on memory parameters.



Traffic Summaries for Faster Analysis

In addition to timing analysis, the Kibra 380 generates performance metrics that are displayed for read, write and power down operations. Bus metrics are tracked per bank, per rank, and per channel to provide insights into overall memory utilization. The error report shows protocol and timing violations with hyperlinks to the error in question. The ability to monitor Quad rank memory DIMMs allows this self-contained solution to provide much of the testing previously performed with costly logic analyzer-based approaches. Validation teams can now use the Kibra 380 DDR3 protocol analyzer to achieve better test coverage at lower overall cost.

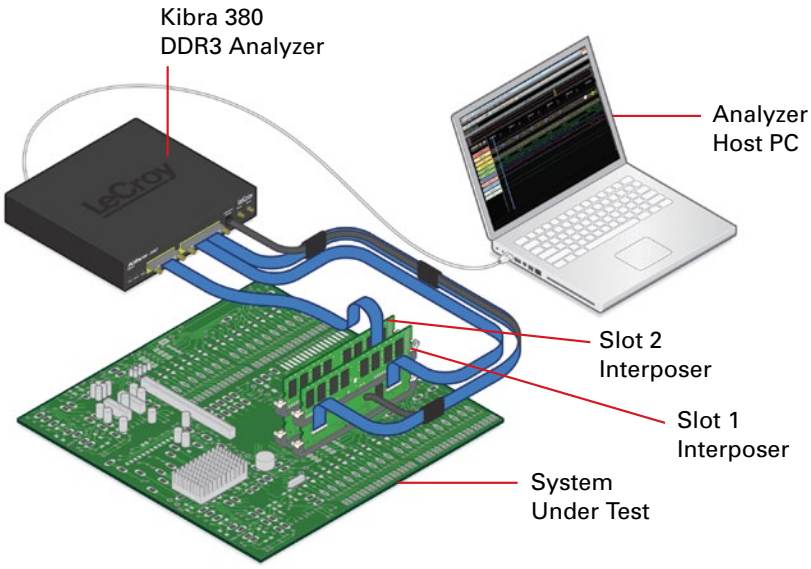


Search for commands by Rank or Bank Address.

SPECIFICATION AND ORDERING INFORMATION

Trigger Out On Read / Write Operations

The Teledyne LeCroy system features real-time trigger-out for Read / Write operations (WE). This dedicated, low latency SMA trigger out uses DQ/DQS relationships to distinguish Read / Write operations on the bus. Separating complex DQ signaling makes it easier to perform electrical layer characterization with an oscilloscope. The Read/Write Trigger can further specify Rank, Bank, Row and Column to isolate problematic operations.



Specifications

Analyzer System Specifications

Host Requirements	Minimum CPU Required is Intel Core 2 Duo Family or Equivalent (Intel's I7 or Higher Recommended); Memory: 4 GB of RAM; Hard Disk: 1 GB of Disk Space (Additional Space for Trace Files); Display: 1600 x 1200 with at Least 24-bit Color Depth
Protocols Supported	DDR3
Recording Memory Size	4 GB
Data Rates Supported	300 MHz – 800 MHz DIMM Clock Speeds
Probe Interface	DDR3 UDIMM, RDIMM Slot Interposer
Front Panel LEDs	Power, Status, Trigger
Front Panel Connectors	Cable Interface to DIMM Slot 1 Interposer, Cable Interface to DIMM Slot 2 Interposer, Read Trigger Output (SMA), Write Trigger Output (SMA), Interposer Probe Power Connector
Trigger Output (SMA)	Write Trigger Output (SMA), Interposer Probe Power Connector
Rear Panel Connectors	CrossSync Connector, USB 2.0 Connection to Host PC: Trigger IN SMA, Trigger OUT SMA External RefClk-IN SMA
Dimensions	(W x H x D) 20 x 3.2 x 23 cm (8" W x 1.25" H x 9" D)
Weight	1.1 Kg (2.8 lbs)
Power Requirements	External 12 V Power
Environmental	Operating 0 to 55 °C (32 to 131 °F), Non-operating -20 to 80 °C (-4 to 176 °F) Humidity 10 to 90% RH (non-condensing)

Probe Specifications

The Kibra 380 includes DDR3 DIMM slot interposer probes that provide the mechanical and electrical interface between the Kibra 380 analyzer and the DDR3 system under test. The system is available with all the necessary probes capable of monitoring two slots of quad rank DDR3 DIMMs operating to 1600 MT/s. The probes operate non-intrusively and introduce less than 90 ps of latency to the DDR3 signal.

Probe Specifications (cont'd)

Compatible with all Standard 240-pin DDR3 SDRAM DIMM's up to 1600 MT/s.
Analysis is Performed on up to 4 Ranks using Channel 1 Slot
Analysis is Performed on up to 8 Ranks when using both Channel 1 and Channel 2 Slots
18" Cable Length between Analyzer and DUT

CrossSync™ Support

CrossSync is the Teledyne LeCroy analyzer synchronization framework that enables time-aligned display of protocol traffic from multiple daisy-chained analyzers. By connecting the built-in sync ports on the Kibra 380 users can monitor multiple memory channels concurrently. The same interface can also be used to synchronize DDR3 operations with bus traffic from other Teledyne LeCroy analyzers including USB, PCI Express, SAS or SATA.

Ordering Information

Product Description	Product Code
Kibra 380 DDR3 Standard Analyzer System (includes DDR3 Analyzer System, DIMM Slot 1 and DIMM Slot 2 Interposer Probes; Two 18" Interposer Ribbon and Power Cables)	DDR-T0S3-D01-X
DDR3 DIMM Slot 1 Interposer Probe Kit	DDR-AC01-D01-X
DDR3 DIMM Slot 2 Interposer Probe Kit	DDR-AC02-D01-X
Mounting Bracket Kit	ACC-BRKT-013-X
DDR3 SMA (m) to SMA (m) Cable Kit 1 M (Qty: 3)	DDR-AC03-D01-X

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Local sales offices are located throughout the world.
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